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Question Paper Code : 52907

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Second/Third Semester

Electronics and Communication Engineering

EC 6302 — DIGITAL ELECTRONICS

(Common to Mechatronics Engineering/Robotics and Automation Engineering)

(Regulation 2013)

(Also common to PTEC 6302 – Digital Electronics for B.E. (Part-Time) – Second Semester – Electronics and Communication Regulation 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How can a X-OR gate be used as an inverter?

2. What is meant by "two level logic"?

3. How an odd parity bit is generated for 4 data bits?

4. What is the minimum number of selection lines required for selecting one output from 'n' input lines?

5. What is the main difference between gated latch and an edge triggered flip-flop?

6. What is meant by "lock-out" problem in counters?

7. Define memory access time.

8. Distinguish between SRAM and DRAM.

9. What is a dynamic hazard and when do they occur?

10. Mention the elements of an Algorithmic State Machine (ASM) chart.

PART B — (5 × 13 = 65 marks)

11. (a) Using Quine-Mc Cluskey method, obtain the minimal POS expression given $f = \pi M$ (0, 1, 4, 5, 9, 11, 13, 15, 16, 17, 25, 27, 28, 29, 31). d(20, 21, 22, 30).

Or

(b) (i) Reduce the following Boolean expressions:

(1) $(x'y' + z)' + z + xy + wz$ to three literals.

(2) $A'B(D' + C'D) + B(A + A'CD)$ to one literal.

(ii) Using K-Map, simplify the given Boolean expression

$A'B'C'D' + A'CD' + AB'D' + ABCD + A'BD$ (7+6)

12. (a) (i) Draw the logic diagram and truth table of a 2 to 4 line decoder with enable input and explain its operation.

(ii) Implement a BCD to Grey code converter using K-maps. (6+7)

Or

(b) (i) Draw the logic diagram of a 2 × 2 binary multiplier and explain its operation. (6+7)

(ii) Design a combinational circuit with 3 inputs x, y and z and 3 outputs A, B and C. The binary input is 0, 1, 2 or 3, the binary output is two greater than the input. Also the binary input is 4, 5, 6 or 7, the binary output is three less than the input?

13. (a) With neat logic diagram and timing diagram, explain the operation of a 3-bit binary ripple up/down counter constructed using JK flip-flop. (13)

Or

(b) (i) With a neat diagram, explain the operation of a 4-bit universal shift register.

(ii) With a neat logic diagram and function table, explain the working of a SR flip-flop. (10+3)

14. (a) Design a combinational circuit using PAL for the following Boolean functions: (13)

w(A,B,C,D) = Σ(2,12,13)

x(A,B,C,D) = Σ(7,8,9,10,11,12,13,14,15)

y(A,B,C,D) = Σ(0,2,3,4,5,6,7,8,10,11,15)

z(A,B,C,D) = Σ(1,2,8,12,13)

Or

(b) (i) Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number.

(ii) With a neat diagram, explain in detail about the working of bipolar SRAM cell. (8+5)

15. (a) (i) By taking a suitable example, briefly explain about the hazards that occur in a combinational circuit and how a hazard free circuit can be designed.

(ii) Obtain the reduced state table for the following state table of an asynchronous sequential circuit. (7+6)

Present state	Next State $x=0$	Next State $x=1$	Output $x=0$	Output $x=1$
a	d	b	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

Or

(b) (i) Write a verilog code to implement a modulo 3 up –down counter. (8)

(ii) What is the advantage of using software packages for designing digital circuits. (5)

PART C — (1 × 15 = 15 marks)

16. (a) A sequential circuit has two JK flip-flops A and B, two inputs x and y and one output z. The flip-flop input equations and circuit output equations are:

$J_A = Bx + B'y'$ $K_A = B'xy'$

$J_B = A'X$ $K_B = A + xy'$

$z = Ax'y' + Bx'y'$

(i) Draw the logic diagram of the circuit

(ii) Tabulate the state table

(iii) Derive the state equations for A and B

Or

(b) Write briefly on FPGA. Compare the advantages of a digital controller using FPGA and using discrete IC devices.

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